AMENDMENTS TO THE CLAIMS

Claim 1-5. (Canceled)

Claim 6. (Previously Presented) A rake receiver circuit for receiving multi-path signals, the rake receiver comprising:

a first rake finger circuit having a first variable delay element, where the first variable delay element is configured to receive a first delay control signal, the first delay control signal value being selected to align a first delay introduced by the first variable delay element with a first multi-path signal to produce a first correlated data signal;

a second rake finger circuit having a second variable delay element, where the second variable delay element is configured to receive a second delay control signal, the second delay control signal value being selected to align a second delay introduced by the second variable delay element with a second multi-path signal to produce a second correlated data signal;

a scan control circuit configured to receive the first and second correlated signals and, responsive thereto, generate the first and second delay control signals, where the scan control circuit is configured to generate the first delay control signal by: (i) varying the first delay control signal over a first predetermined range of values, (ii) measuring a signal power level of the first correlated data signal to determine a value of the first delay control signal corresponding to a highest measured signal power level of the first correlated data signal, and (iii) setting the first delay control signal to the value of the first delay control signal corresponding to the highest measured signal power level of the first correlated data signal for operation, and where the scan control circuit is further configured to generate the second delay control signal by: (i) varying the second delay control signal over a second predetermined range of values, (ii) measuring a signal

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power level of the second correlated data signal to determine a value of the second delay control signal corresponding to a highest measured signal power level of the second correlated data signal, and (iii) setting the second delay control signal to the value of the second delay control signal corresponding to the highest measured signal power level of the second correlated data signal for operation; and

a summing circuit for summing the first and second correlated signals to produce a combined data signal.

Claims 7-8. (Canceled)

Claim 9. (Previously Presented) The rake receiver of Claim 6, where the scan control circuit is further configured to generate the first and second delay control signals responsive to a scan control signal.

Claims 10-17. (Canceled)

Claim 18. (Previously Presented) The rake receiver of claim 6, wherein the first delay and the second delay are selected so that the first correlated data signal and the second correlated data signal arrive at the summing circuit at substantially the same time.

Claim 19. (New) The rake receiver of claim 6, wherein the scan control circuit is configured to generate the first delay control signal by varying the first delay control signal over the first

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predetermined range of values, wherein the first predetermined range of values approximately corresponds to an amount of time for the first multi-path signal to travel to the rake receiver.

Claim 20. (New) The rake receiver of claim 6, wherein the first rake finger circuit includes a multiplier in series with a variable delay element and a phase adjuster.

Claim 21. (New) The rake receiver of claim 20, wherein the multiplier multiplies a PN code with the first multi-path signal to generate a first decoded signal.

Claim 22. (New) The rake receiver of claim 21, wherein the variable delay element delays the first decoded signal according to the first delay control signal to produce a first delayed decoded signal.

Claim 23. (New) The rake receiver of claim 22, wherein the phase adjuster adjusts the phase of the first delayed decoded signal.

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